



The diagram illustrates a 4-to-1 multiplexer implemented using 74LS00 NAND gates. It consists of three stages of logic:

- Stage 1 (AND Gates):** Four 2-input AND gates. The first two take inputs SET 1 (1), ENABLE (12), and CLOCK (13) and SET 2 (9), ENABLE (10), and CLOCK (11). The next two take inputs RESET 1 (2), ENABLE (3) and RESET 2 (4), ENABLE (5).
- Stage 2 (OR Gates):** Two 2-input OR gates. The first OR gate takes the outputs of the first two AND gates. The second OR gate takes the outputs of the last two AND gates.
- Stage 3 (NAND Gates):** Two 74LS00 NAND gates. The first NAND gate takes the output of the first OR gate and the output of the first AND gate (RESET 1 AND ENABLE). The second NAND gate takes the output of the second OR gate and the output of the second AND gate (RESET 2 AND ENABLE).

The final outputs are labeled 1, 2, 3, 4, 5, 6, 7, and 8.

Warning
Pinout may vary between families.
74S51 or 7451 may vary from 74LS51.

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