

LM1203

LM1203 RGB Video Amplifier System



Literature Number: SNOSC07A

LM1203 RGB Video Amplifier System

General Description

The LM1203 is a wideband video amplifier system intended for high resolution RGB color monitor applications. In addition to three matched video amplifiers, the LM1203 contains three gated differential input black level clamp comparators for brightness control and three matched attenuator circuits for contrast control. Each video amplifier contains a gain set or "Drive" node for setting maximum system gain ($A_v = 4$ to 10) as well as providing trim capability. The LM1203 also contains a voltage reference for the video inputs. For high resolution monochrome monitor applications see the LM1201 Video Amplifier System datasheet.

Features

- Three wideband video amplifiers (70 MHz @ -3dB)
- Inherently matched (± 0.1 dB or 1.2%) attenuators for contrast control
- Three externally gated comparators for brightness control
- Provisions for independent gain control (Drive) of each video amplifier
- Video input voltage reference
- Low impedance output driver

Block and Connection Diagram

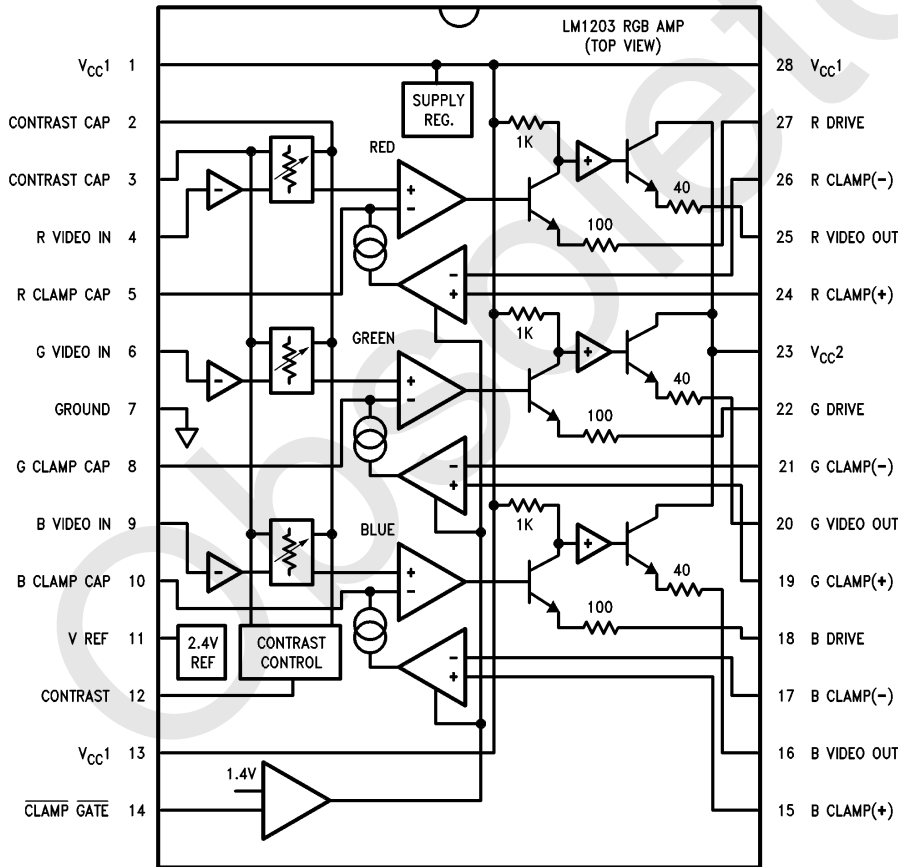


FIGURE 1
Order Number LM1203N
See NS Package Number NA28F

TL/H/9178-1

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC} Pins 1, 13, 23, 28 (Note 1)	13.5V
Voltage at Any Input Pin, V_{IN}	$V_{CC} \geq V_{IN} \geq GND$
Video Output Current, I16, 20 or 25	28 mA
Power Dissipation, P_D (Above 25°C) Derate Based on θ_{JA} and T_J	2.5W
Thermal Resistance, θ_{JA}	50°C/W
Junction Temperature, T_J	150°C

Storage Temperature Range, T_{STG}	-65°C to +150°C
Lead Temperature, (Soldering, 10 sec.)	265°C
ESD susceptibility	1 kV
Human body model: 100 pF discharged through a 1.5 k Ω resistor	

Operating Ratings (Note 9)

Temperature Range	0°C to 70°C
Supply Voltage (V_{CC})	$10.8V \leq V_{CC} \leq 13.2V$

Electrical Characteristics

 See Test Circuit (Figure 2), $T_A = 25^\circ\text{C}$; $V_{CC1} = V_{CC2} = 12V$

DC Static Tests

 S17, 21, 26 Open; V12 = 6V; V14 = 0V; V15 = 2.0V unless otherwise stated

Label	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
I _s	Supply Current	V_{CC} 1 only	73	90.0		mA(max)
V11	Video Input Reference Voltage		2.4	2.2		V(min)
				2.6		V(max)
I _b	Video Input Bias Current	Any One Amplifier	5.0	20		μA (max)
V14 l	Clamp Gate Low Input Voltage	Clamp Comparators On	1.2	0.8		V(max)
V14 h	Clamp Gate High Input Voltage	Clamp Comparators Off	1.6	2.0		V(min)
I14 l	Clamp Gate Low Input Current	V14 = 0V	-0.5	-5.0		μA (max)
I14 h	Clamp Gate High Input Current	V14 = 12V	0.005	1		μA (max)
I _{clamp+}	Clamp Cap Charge Current	V5, 8 or 10 = 0V	850	500		μA (min)
I _{clamp-}	Clamp Cap Discharge Current	V5, 8 or 10 = 5V	-850	-500		μA (min)
V _{ol}	Video Output Low Voltage	V5, 8 or 10 = 0V	0.9	1.25		V(max)
V _{oh}	Video Output High Voltage	V5, 8 or 10 = 5V	8.9	8.2		V(min)
$\Delta V_o(2V)$	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 2V	± 0.5	± 50		mV(max)
$\Delta V_o(4V)$	Video Output Offset Voltage	Between Any Two Amplifiers V15 = 4V	± 0.5	± 50		mV(max)

AC Dynamic Tests

 S17, 21, 26 Closed; V14 = 0V; V15 = 4V; unless otherwise stated

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units (Limits)
A _v max	Video Amplifier Gain	V12 = 12V, $V_{IN} = 560 \text{ mVp-p}$	6.0	4.5		V/V(min)
$\Delta A_v 5V$	Attenuation @ 5V	Ref: A _v max, V12 = 5V	-10			dB
$\Delta A_v 2V$	Attenuation @ 2V	Ref: A _v max, V12 = 2V	-40			dB
A _v match	Absolute gain match @ A _v max	V12 = 12V (Note 5)	± 0.5			dB
$\Delta A_v \text{ track1}$	Gain change between amplifiers	V12 = 5V (Notes 5, 8)	± 0.1		± 0.5	dB(max)
$\Delta A_v \text{ track2}$	Gain change between amplifiers	V12 = 2V (Notes 5, 8)	± 0.3		± 0.7	dB(max)
THD	Video Amplifier Distortion	V12 = 3V, $V_O = 1 \text{ Vp-p}$	0.5			%
f (-3 dB)	Video Amplifier Bandwidth (Notes 4, 6)	V12 = 12V, $V_O = 100 \text{ mV}_{\text{rms}}$	70			MHz
t _r	Output Rise Time (Note 4)	$V_O = 4 \text{ Vp-p}$	5			ns
t _f	Output Fall Time (Note 4)	$V_O = 4 \text{ Vp-p}$	7			ns

AC Dynamic Tests $S_{17}, 21, 26$ Closed; $V_{14} = 0V$; $V_{15} = 4V$; unless otherwise stated (Continued)

Symbol	Parameter	Conditions	Typ	Tested Limit (Note 2)	Design Limit (Note 3)	Units
Vsep 10 kHz	Video Amplifier 10 kHz Isolation	$V_{12} = 12V$ (Note 7)	-65			dB
Vsep 10 MHz	Video Amplifier 10 MHz Isolation	$V_{12} = 12V$ (Notes 4, 7)	-46			dB

Note 1: V_{CC} supply pins 1, 13, 23, 28 must be externally wired together to prevent internal damage during V_{CC} power on/off cycles.

Note 2: These parameters are guaranteed and 100% production tested.

Note 3: Design limits are guaranteed (but not 100% production tested). These limits are not used to calculate outgoing quality levels.

Note 4: When measuring video amplifier bandwidth or pulse rise and fall times, a double sided full ground plane printed circuit board without socket is recommended. Video Amplifier 10 MHz isolation test also requires this printed circuit board.

Note 5: Measure gain difference between any two amplifiers. $V_{IN} = 1 V_{p-p}$.

Note 6: Adjust input frequency from 10 kHz (A_{vmax} ref level) to the -3 dB corner frequency ($f - 3$ dB).

Note 7: Measure output levels of the other two undriven amplifiers relative to driven amplifier to determine channel separation. Terminate the undriven amplifier inputs to simulate generator loading. Repeat test at $f_{IN} = 10$ MHz for $V_{sep} = 10$ MHz.

Note 8: ΔA_v track is a measure of the ability of any two amplifiers to track each other and quantifies the matching of the three attenuators. It is the difference in gain change between any two amplifiers with the Contrast Voltage V_{12} at either 5V or 2V measured relative to an A_v max condition $V_{12} = 12V$. For example, at A_v max the three amplifiers gains might be 17.4 dB, 16.9 dB, and 16.4 dB and change to 7.3 dB, 6.9 dB, and 6.5 dB respectively for $V_{12} = 5V$. This yields the measured typical ± 0.1 dB channel tracking.

Note 9: Operating Ratings indicate conditions for which the device is functional. See Electrical Specifications for guaranteed performance limits.

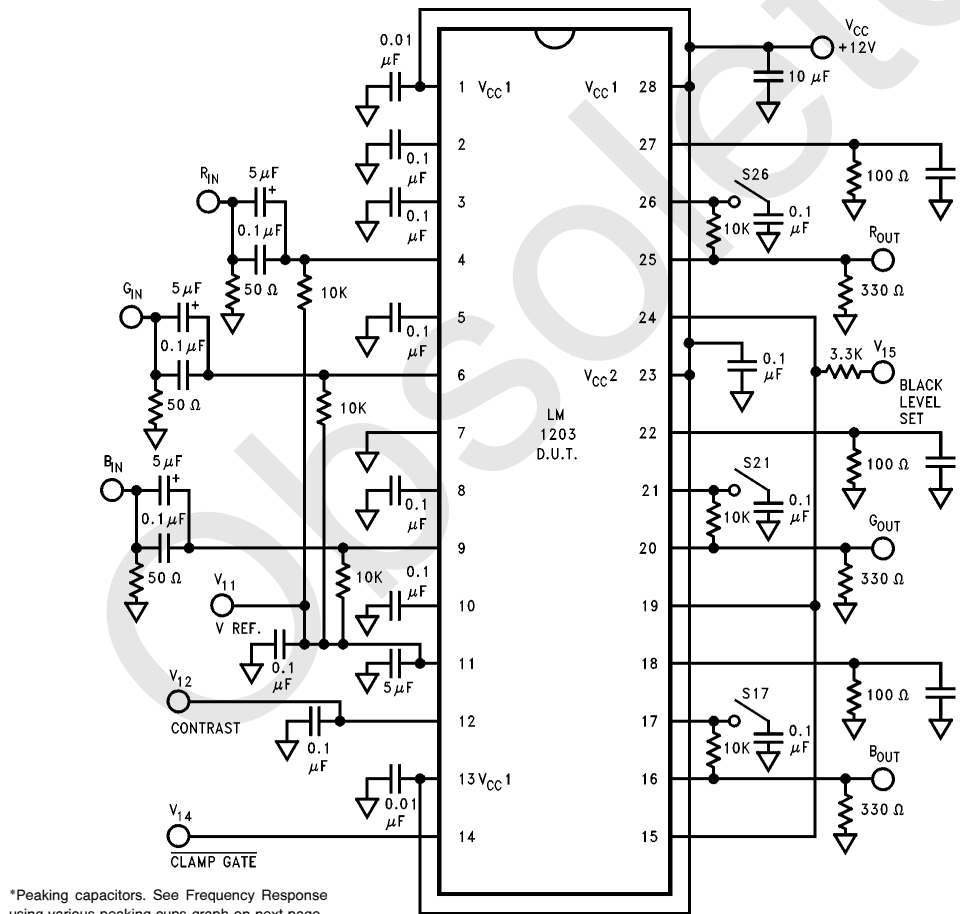
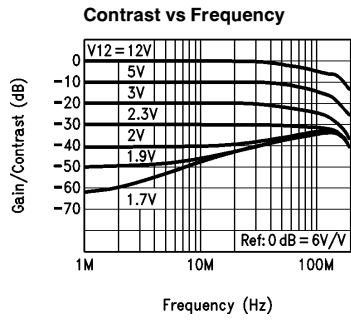


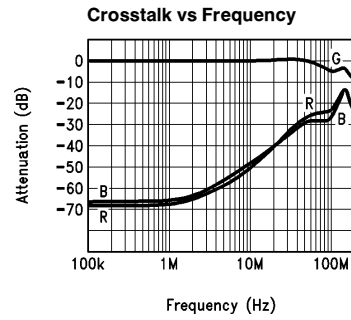
FIGURE 2. LM1203 Test Circuit

TL/H/9178-2

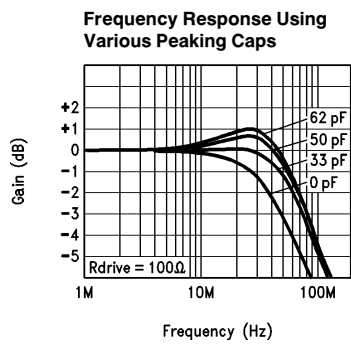
Typical Performance Characteristics



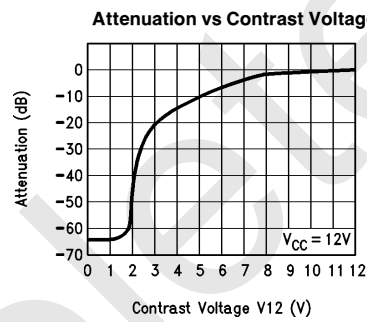
TL/H/9178-11



TL/H/9178-12

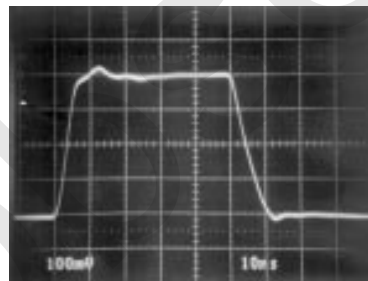


TL/H/9178-13



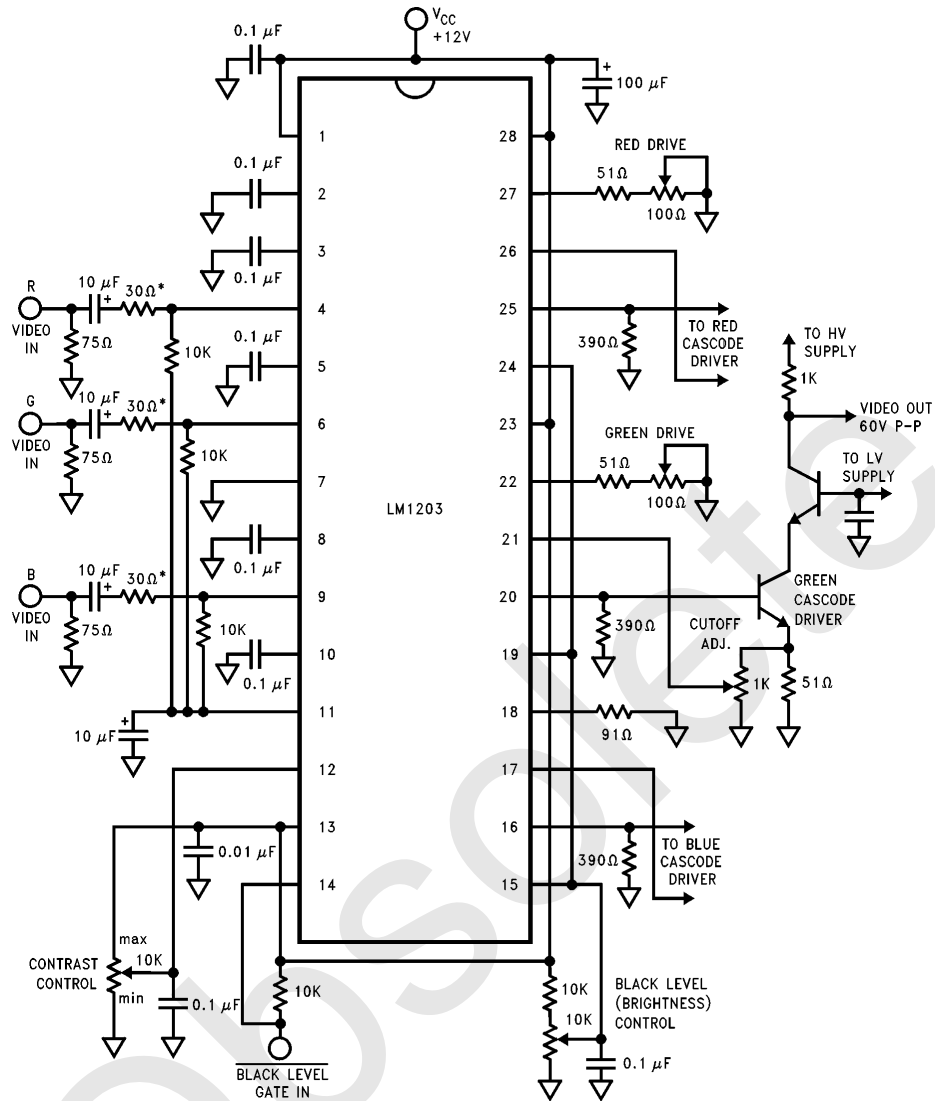
TL/H/9178-14

Pulse Response



Rise & Fall Times
Vert. = 1V/Div.
Horiz. = 10 ns/Div.

-- GND
TL/H/9178-15



TL/H/9178-3

FIGURE 3. LM1203 Typical Application

* 30Ω resistors are added to the input pins for protection against current surges coming through the 10 µF input capacitors. By increasing these resistors to well over 100Ω the rise and fall times of the LM1203 can be increased for EMI considerations.

Applications Information

Figure 4 shows the block diagram of a typical analog RGB color monitor. The RGB monitor is used with CAD/CAM work stations, PC's, arcade games and in a wide range of other applications that benefit from the use of color display terminals. The RGB color monitor characteristics may differ in such ways as sweep rates, screen size, CRT color trio spacing (dot pitch), or in video amplifier bandwidths but will still be generally configured as shown in Figure 4. Separate horizontal and vertical sync signals may be required or they may be contained in the green video input signal. The video input signals are usually supplied by coax cable which is terminated in 75Ω at the monitor input and internally ac cou-

pled to the video amplifiers. These input signals are approximately 1 volt peak to peak in amplitude and at the input of the high voltage video section, approximately 6V peak to peak. At the cathode of the CRT the video signals can be as high as 60V peak to peak. One important requirement of the three video amplifiers is that they match and track each other over the contrast and brightness control range. The Figure 4 block labeled "VIDEO AMPLIFICATION WITH GAIN AND DC CONTROL" describes the function of the LM1203 which contains the three matched video amplifiers, contrast control and brightness control.

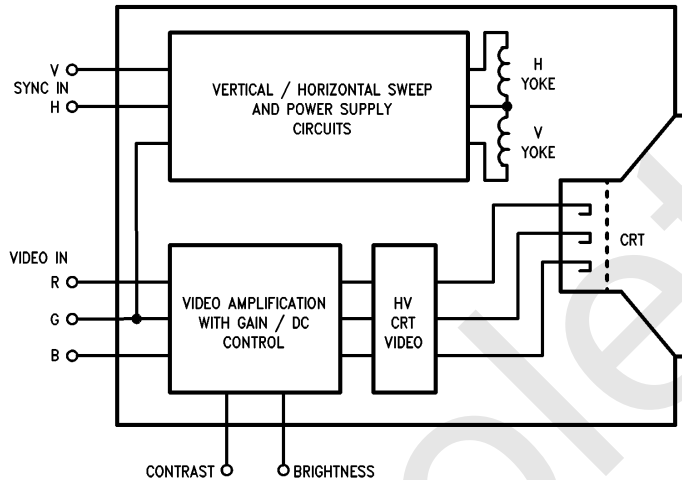


FIGURE 4. Typical RGB Color Monitor Block Diagram

TL/H/9178-4

Circuit Description

Figure 5 is a block diagram of one of the video amplifiers along with the contrast and brightness controls. The contrast control is a dc-operated attenuator which varies the ac gain of all three amplifiers simultaneously while not introducing any signal distortions or tracking errors. The brightness control function requires a "sample and hold" circuit (black level clamp) which holds the dc bias of the video amplifiers and CRT cathodes constant during the black level reference portion of the video waveform. The clamp comparator, when gated on during this reference period, will charge or discharge the clamp capacitor until the plus input of the clamp comparator matches that of the minus input voltage which was set by the brightness control.

Figure 6 is a simplified schematic of one of the three video amplifiers along with the recommended external components. The IC pin numbers are circled with all external components shown outside of the dashed line. The video input is applied to pin 6 via the 10 μF coupling capacitor. DC bias

to the video input is through the 10 k Ω resistor which is connected to the 2.4V reference at pin 11. The low frequency roll-off of the amplifier is set by these two components. Transistor Q1 buffers the video signal to the base of Q2. The Q2 collector current is then directed to the V_{CC} 1 supply directly or through the 1k load resistor depending upon the differential DC voltage at the bases of Q3 and Q4. The Q3 and Q4 differential base voltage is determined by the contrast control circuit which is described below. RF decoupling capacitors are required at pins 2 and 3 to insure high frequency isolation between the three video amplifiers which share these common connections. The black level dc voltage at the collector of Q4 is maintained by Q5 and Q6 which are part of the black level clamp circuit also described below. The video signal appearing at the collector of Q4 is then buffered by Q7 and level shifted down by Z1 and Q8 to the base of Q9 which will then provide additional system gain.

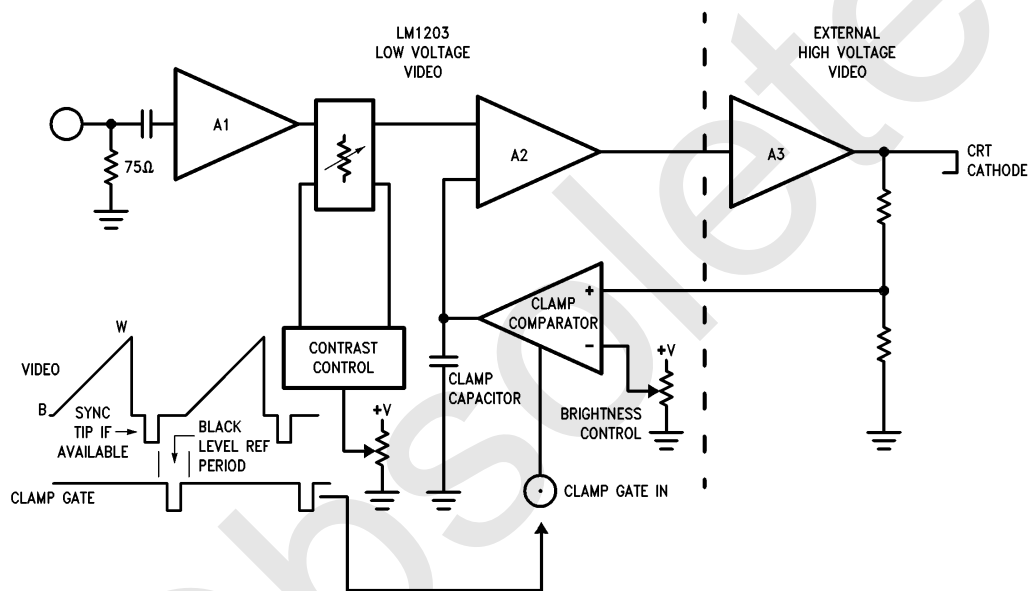


FIGURE 5. Block Diagram of LM1203 Video Amplifier with Contrast and Black Level Control

TL/H/9178-5

Circuit Description (Continued)

TL/H/9178-6

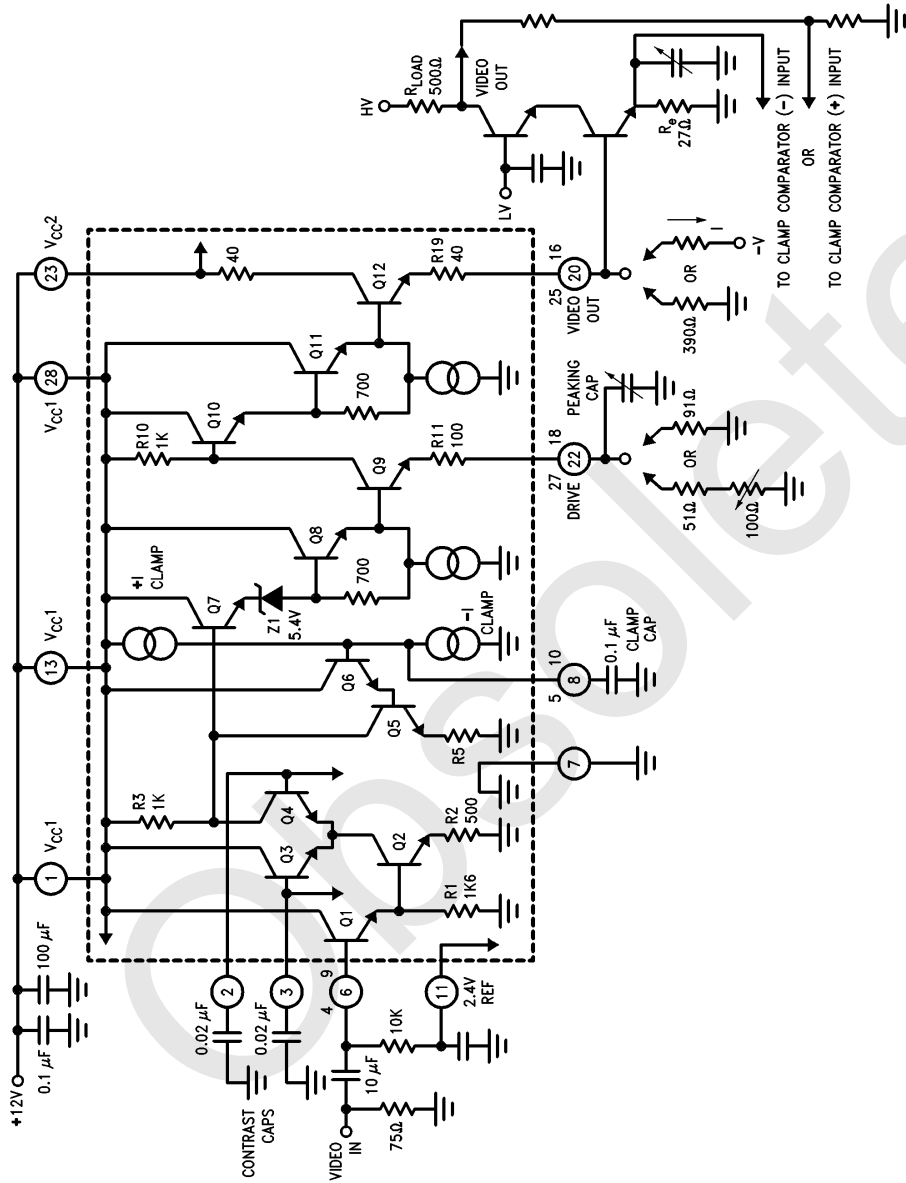


FIGURE 6. Simplified LM1203 Video Amplifier Section with Recommended External Components

Circuit Description (Continued)

The "Drive" pin will allow the user to trim the Q9 gain of each amplifier to correct for differences in the CRT and high voltage cathode driver gain stages. A small capacitor (33 pF) at this pin will extend the high frequency gain of the video amplifier by compensating for some of the internal high frequency roll off. To use this capacitor and still provide variable gain adjustment, the 51Ω and series 100Ω pot should be used with the red and green drive pins. The 91Ω resistor used with the blue drive pin will set the system gain to approximately 6.2 and allow adjustment of the red and green gains to 6.2 plus or minus 25%. The video signal at the collector of Q9 is buffered and level shifted down by Q10 and Q11 to the base of the output emitter follower Q12. Between the emitter of Q12 and the video output pin is a 40Ω resistor which was included to prevent spurious oscillations when driving capacitive loads. An external emitter resistor must be added between the video output pin and ground. The value of this resistor should not be less than 390Ω or package power limitations may be exceeded when worst case (high supply, max supply current, max temp) calculations are made. If negative going pulse slewing is a problem because of high capacitive loads (> 10 pF), a more efficient method of emitter pull down would be to connect a suitable resistor to a negative supply voltage. This has the effect of a current source pull down when the minus supply voltage is -12V and the emitter current is approximately

10 mA. The system gain will also increase slightly because less signal will be lost across the internal 40Ω resistor. Precautions must be taken to prevent the video output pin from going below ground because IC substrate currents may cause erratic operation. The collector currents from the video output transistors are returned to the power supply at V_{CC} 2 pin 23. When making power dissipation calculations note that the data sheet specifies only the V_{CC} 1 supply current at 12V. The IC power dissipation contribution of V_{CC} 2 is dependent upon the video output emitter pull down load.

In applications that require video amplifier shut down because of fault conditions detected by monitor protection circuits, pin 11 and the wiper arms of the contrast and brightness controls can be grounded without harming the IC. This assumes some series resistance between the top of the control pots and V_{CC}.

Figure 7 shows the internal construction of the pin 11 2.4V reference circuit which is used to provide temperature and supply voltage tracking compensation for the video amplifier inputs. The value of the external DC biasing resistors should not be larger than 10 kΩ because minor differences in input bias currents to the individual video amplifiers may cause offsets in gain.

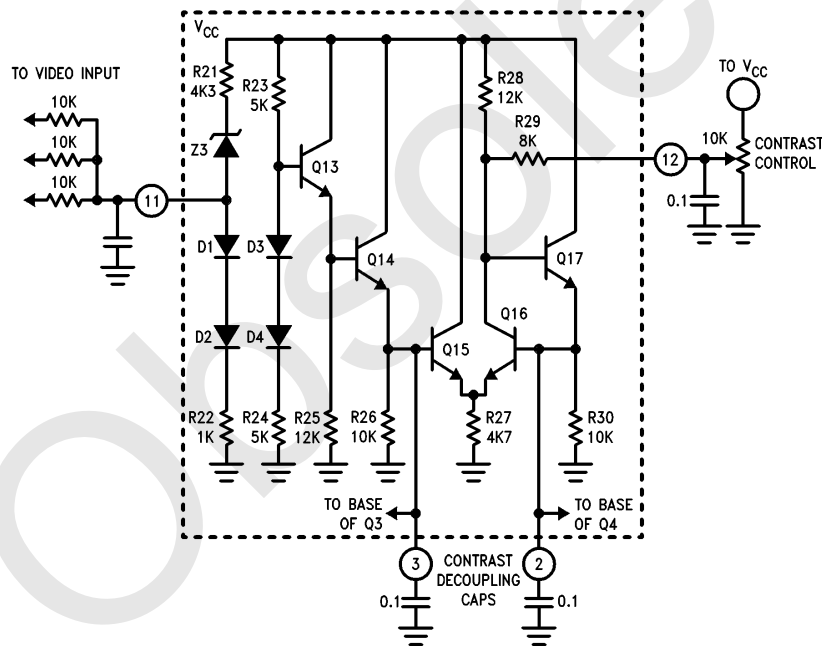


FIGURE 7. LM1203 Video Input Voltage Reference and Contrast Control Circuits

TL/H/9178-7

Circuit Description (Continued)

Figure 7 also shows how the contrast control circuit is configured. Resistors R23, 24, diodes D3, 4 and transistor Q13 are used to establish a low impedance zero TC half supply voltage reference at the base of Q14. The differential amplifier formed by Q15, 16 and feedback transistor Q17 along with resistors R27, 28 establish a differential base voltage for Q3 and Q4 in Figure 6. When externally adding or subtracting current from the collector of Q16, a new differential voltage is generated that reflects the change in the ratio of currents in Q15 and Q16. To provide voltage control of the Q16 current, resistor R29 is added between the Q16 collector and pin 12. A capacitor should be added from pin 12 to ground to prevent noise from the contrast control pot from entering the IC.

Figure 8 is a simplified schematic of the clamp gate and clamp comparator sections of the LM1203. The clamp gate circuit consists of a PNP input buffer transistor (Q18), a PNP emitter coupled pair referenced on one side to 2.1V (Q19, 20) and an output switch (Q21). When the clamp gate input at pin 14 is high ($>1.5V$) the Q21 switch is on and shunts

the 11 850 μA current to ground. When pin 14 is low ($<1.3V$) the Q21 switch is off and the 11 850 μA current source is mirrored or "turned around" by reference diode D5 and Q26 to provide a 850 μA current source for the clamp comparator(s). The inputs to the comparator are similar to the clamp gate input except that an NPN emitter coupled pair is used to control the current which will charge or discharge the clamp capacitors at pins 5, 8, or 10. PNP transistors are used at the inputs because they offer a number of advantages over NPNs. PNP's will operate with base voltages at or near ground and will usually have a greater reverse emitter base breakdown voltage (BVebo). Because the differential input voltage to the clamp comparator during the video scan period could be greater than the BVebo of NPN transistors a resistor (R34) with a value one half that of R33 or R35 is connected between the bases of Q23 and Q27. This resistor will limit the maximum differential input to Q24, 25 to approximately 350 mV. The clamp comparator common mode range is from ground to approximately 9V and the maximum differential input voltage is V_{CC} and ground.

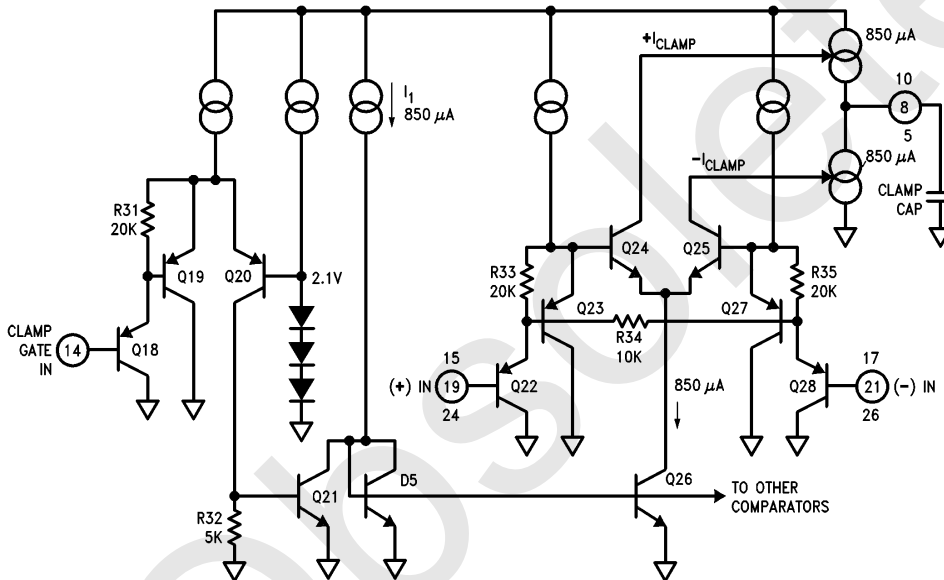


FIGURE 8. Simplified Schematic of LM1203 Clamp Gate and Clamp Comparator Circuits

TL/H/9178-8

Additional Applications of the LM1203

Figure 9 shows how the LM1203 can be set up as a video buffer which could be used in low cost video switcher applications. Pin 14 is tied high to turn off the clamp comparators. The comparator input pins should be grounded as shown. Sync tip (black level if sync is not included) clamping is provided by diodes at the amplifier inputs. Note that the clamp cap pins are tied to the Pin 11 2.4V reference. This was done, along with the choice of 200Ω for the drive pin resistor, to establish an optimum DC output voltage. The

contrast control (Pin 12) will provide the necessary gain or attenuation required for channel balancing. Changing the contrast control setting will cause minor DC shifts at the amplifier output which will not be objectionable as the output is AC coupled to the load. The dual NPN/PNP emitter follower will provide a low impedance output drive to the AC coupled 75Ω output impedance setting resistor. The dual $500\mu\text{F}$ capacitors will set the low frequency response to approximately 4 Hz.

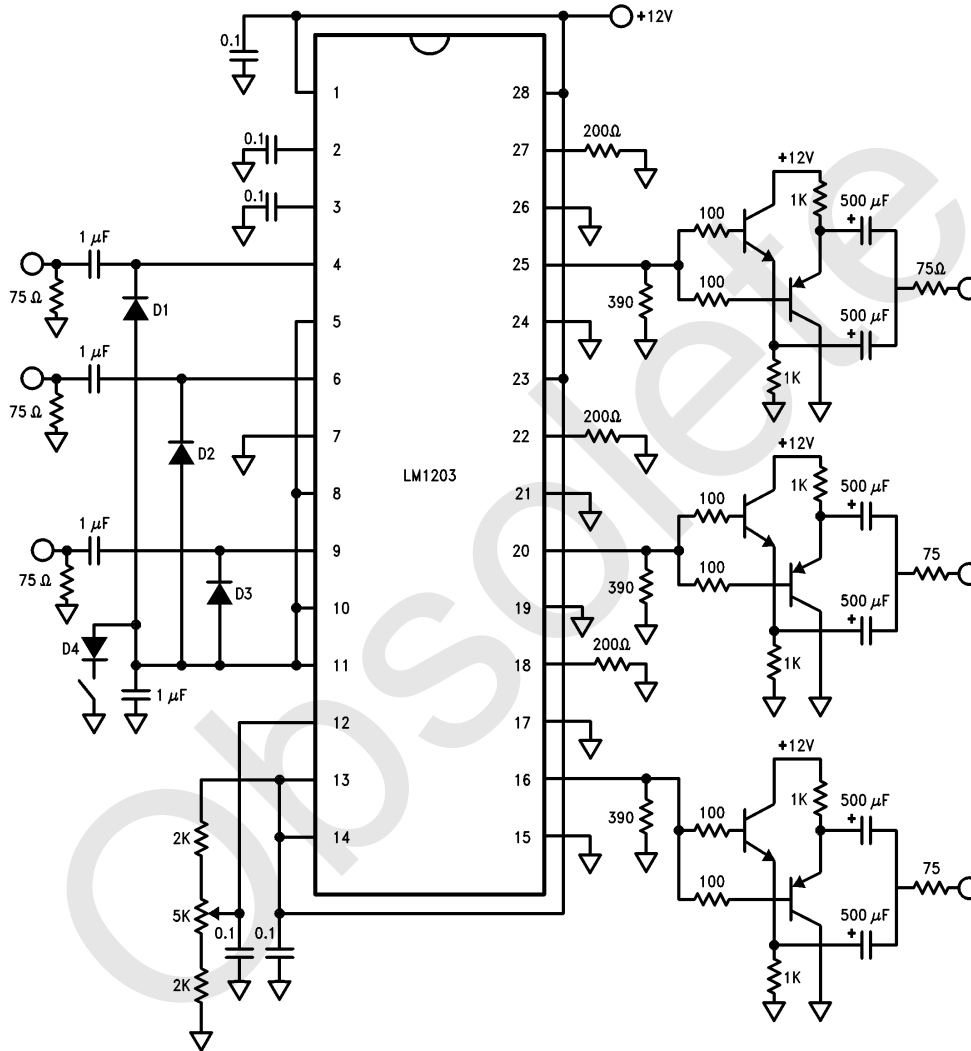


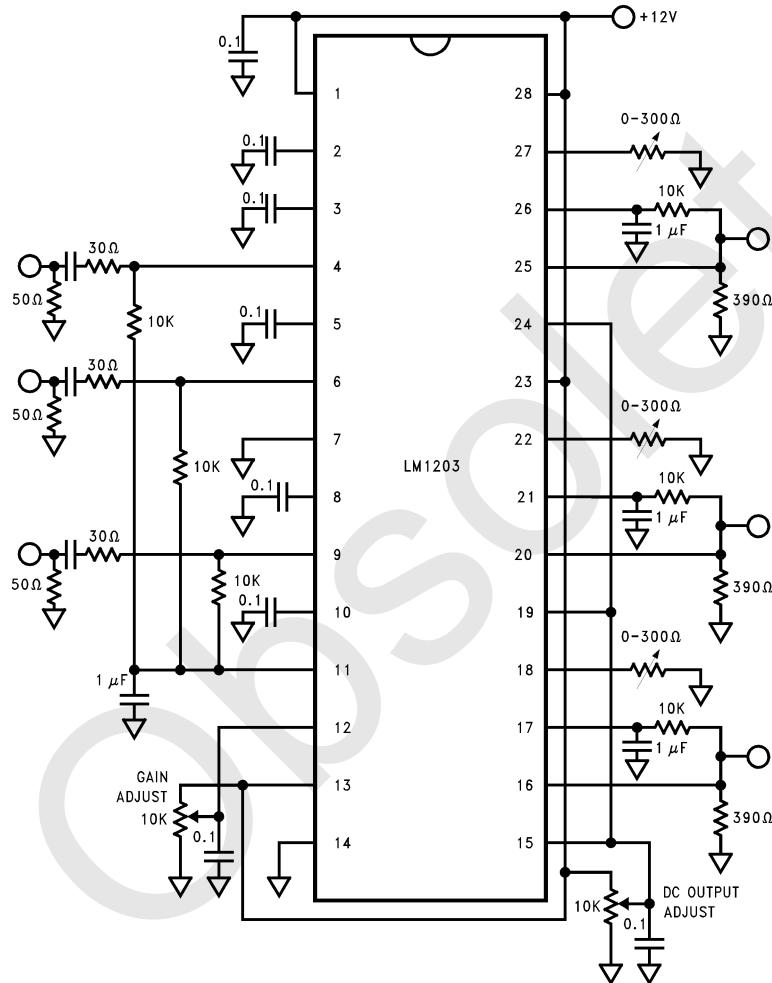
FIGURE 9. RGB Video Buffer with Diode Sync Tip Clamps and 75Ω Cable Driver

TL/H/9178-9

Additional Applications of the LM1203 (Continued)

When diode D4 at Pin 11 is switched to ground the input video signals will be DC shifted down and clamped at a voltage near ground (approximately 250 mV). This will disable the video amplifiers and force the output DC level low. The DC outputs from other similarly configured LM1203s could override this lower DC level and provide the output signals to the 75Ω cable drivers. In this case any additional LM1203s would share the same 390Ω output resistor. The maximum DC plus peak white output voltage should not be allowed to exceed 7V because the "off" amplifier output stage could suffer internal zener damage. See *Figure 3* and text for a description of the internal configuration of the video amplifier.

Figure 10 shows the configuration for a three channel high frequency amplifier with non gated DC feedback. Pin 14 is tied low to turn on the clamp comparators (feedback amplifiers). The inverting inputs (Pins 17, 21, 26) are connected to the amplifier outputs from a low pass filter. Additional low frequency filtering is provided by the clamp caps. The drive resistors can be made variable or fixed at values between 0 and 300Ω. Maximum output swings are achieved when the DC output is set to approximately 4V. The high frequency response will be dependent upon external peaking at the drive pins.



TL/H/9178-10

FIGURE 10. Three Channel High Frequency Amplifier with Non-gated DC Feedback (Non-video Applications)

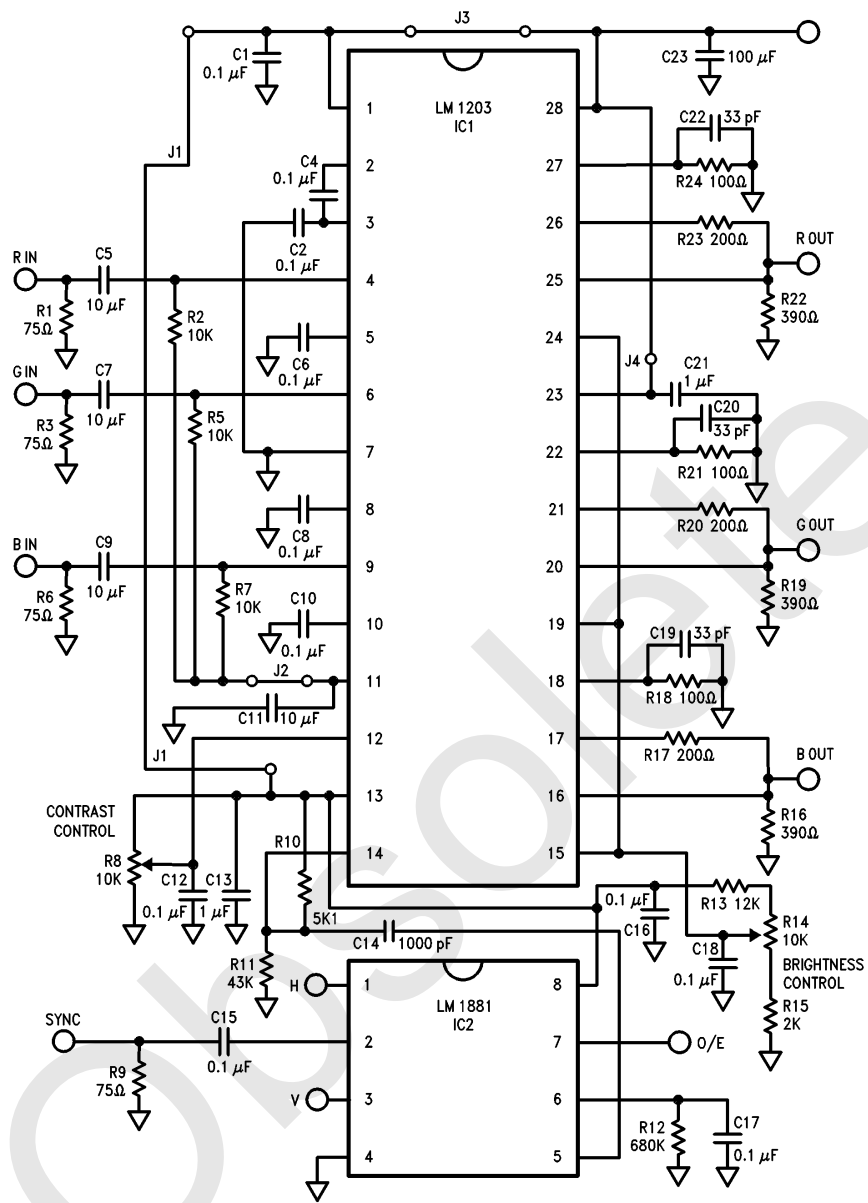
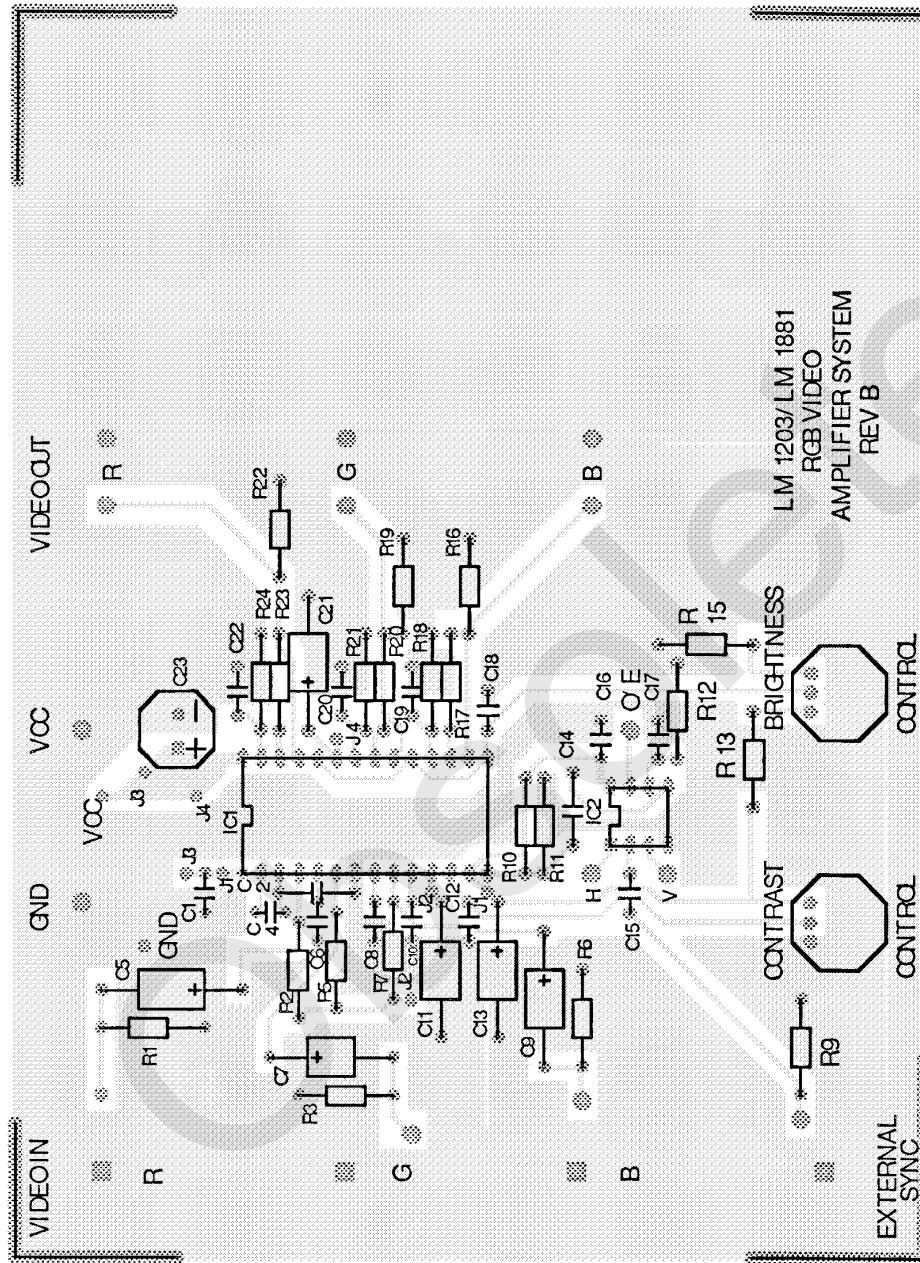


FIGURE 11. LM1203/LM1881 Application Circuit for PC Board

TL/H/9178-16

PC Board with Components

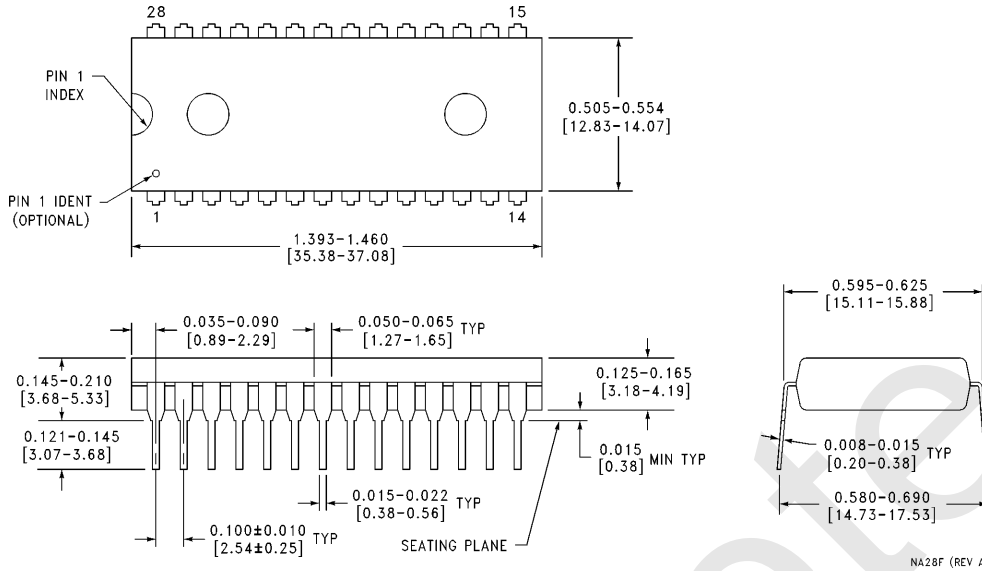


TU/H/9178-17

Obsolete

Physical Dimensions inches (millimeters) unless otherwise noted

Lit. # 107315



28-Lead Molded Dual-In-Line Package (N)
Order Number LM1203N
NS Package Number NA28F

NA28F (REV A)

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: (800) 272-9959
 Fax: (800) 737-7018

<http://www.national.com>

National Semiconductor Europe

Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 180-530 85 85
 English Tel: +49 (0) 180-532 78 32
 Français Tel: +49 (0) 180-532 93 58
 Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.

19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.

Tel: 81-043-299-2308
 Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Mobile Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Transportation and Automotive	www.ti.com/automotive
Video and Imaging	www.ti.com/video

TI E2E Community Home Page

e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2011, Texas Instruments Incorporated